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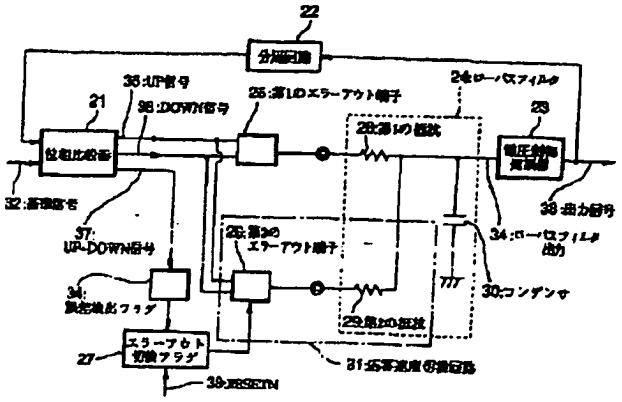
TITLE : HIGH-SPEED LOCK-UP PLL CIRCUIT



ABSTRACT : PROBLEM TO BE SOLVED: To provide a high-speed lock-up PLL circuit capable of switching a high-speed response/a low-speed response within an optional error range and preventing characteristic degradation at the time of changeover.

SOLUTION: Relating to this PLL circuit provided with a voltage controlled oscillator 23, a phase comparator 21, plural error out terminals for outputting the signals of the phase comparator 21 and a low-pass filter 24 for inputting the output of the error out terminals, an error detection flag 34 capable of observing error signals outputted from the phase comparator 21 and an error out changeover flag 27 for turning at least one or more of the plural error out terminals to a high impedance fixed state are provided. The error out changeover flag 27 changes the output of the error out terminal as an object to the high impedance fixed state only when the output of all the error out terminals is high impedance.